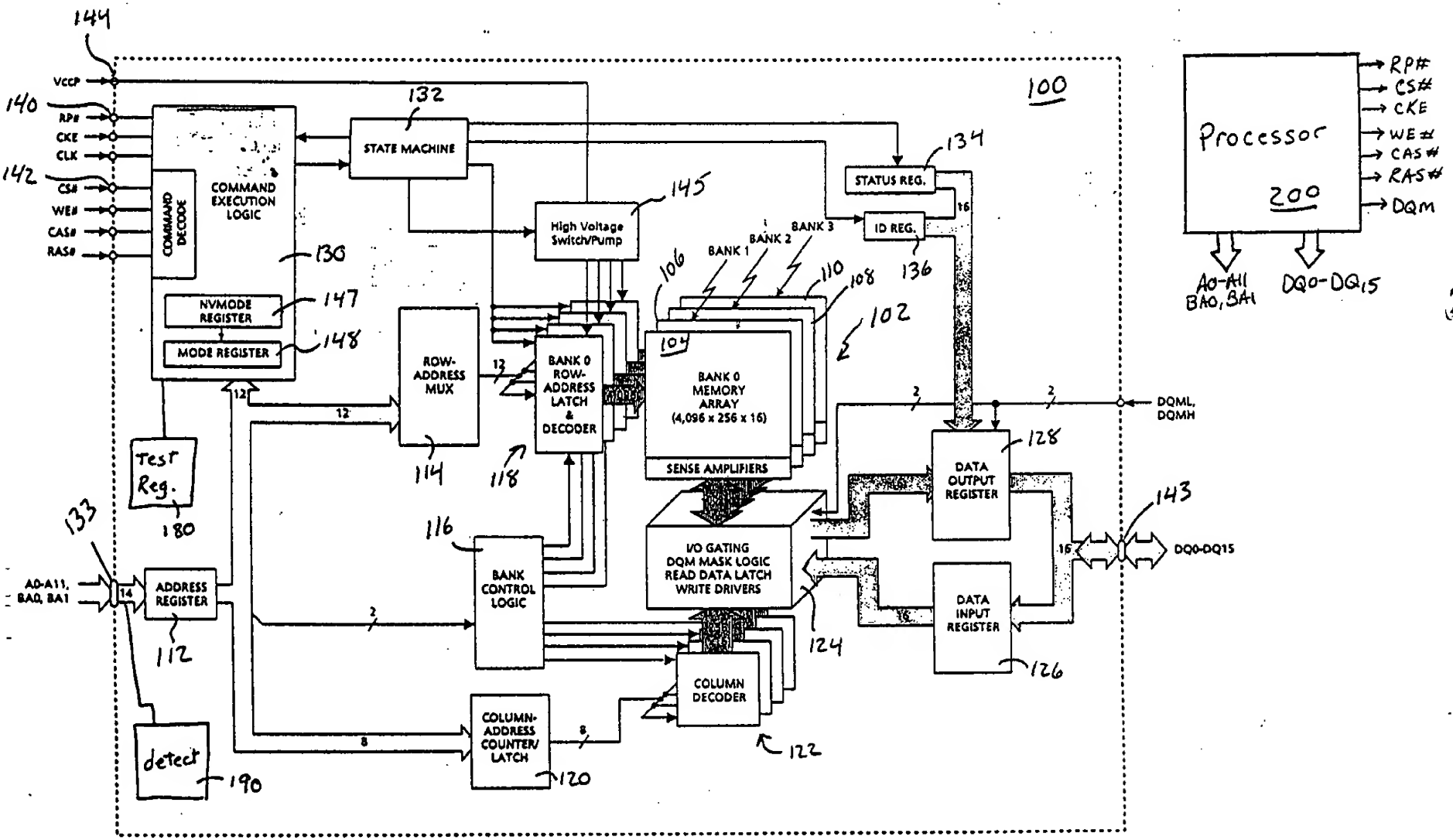
144
VCCP
140
RP#
CKE
CLK
142
CS#
WE#
CAS#
RAS#
COMMAND DECODE
COMMAND EXECUTION LOGIC
130
132
STATE MACHINE
NVMODE REGISTER
147
MODE REGISTER
148
Test Reg.
180
133
A0-A11, BA0, BA1
14
ADDRESS REGISTER
112
detect
190
12
ROW-ADDRESS MUX
114
118
BANK 0 ROW-ADDRESS LATCH & DECODER
BANK 0 MEMORY ARRAY (4,096 x 256 x 16)
SENSE AMPLIFIERS
104
106
BANK 1
BANK 2
BANK 3
110
108
102
116
BANK CONTROL LOGIC
I/O GATING DQM MASK LOGIC READ DATA LATCH WRITE DRIVERS
124
COLUMN DECODER
122
COLUMN-ADDRESS COUNTER/ LATCH
120
8
2
145
High Voltage Switch/Pump
134
STATUS REG.
16
ID REG.
136
100
Processor
200
RP#
CS#
CKE
WE#
CAS#
RAS#
DQM
A0-A11 BA0, BA1
DQ0-DQ15
DQML, DQMH
128
DATA OUTPUT REGISTER
143
DQ0-DQ15
DATA INPUT REGISTER
126

Fig. 1

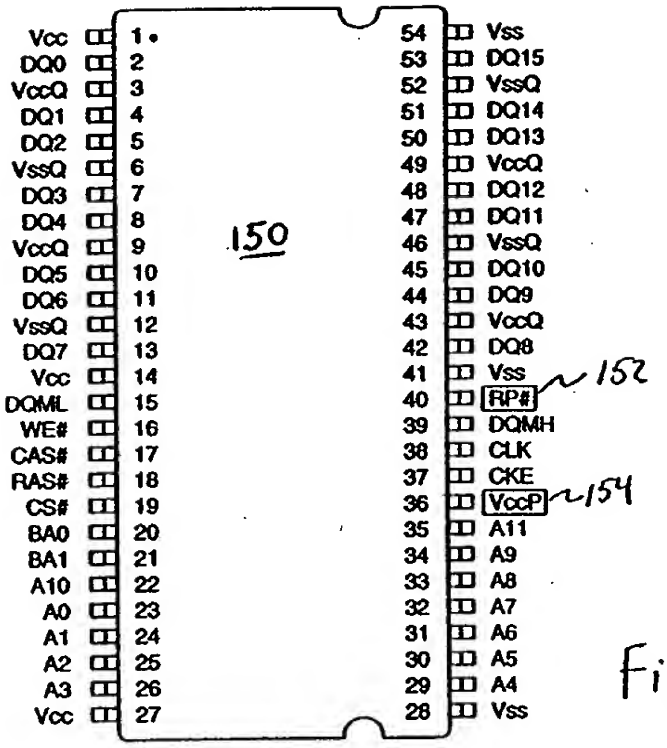
Vcc 1
DQ0 2
VccQ 3
DQ1 4
DQ2 5
VssQ 6
DQ3 7
DQ4 8
VccQ 9
DQ5 10
DQ6 11
VssQ 12
DQ7 13
Vcc 14
DQML 15
WE# 16
CAS# 17
RAS# 18
CS# 19
BA0 20
BA1 21
A10 22
A0 23
A1 24
A2 25
A3 26
Vcc 27
54 Vss
53 DQ15
52 VssQ
51 DQ14
50 DQ13
49 VccQ
48 DQ12
47 DQ11
46 VssQ
45 DQ10
44 DQ9
43 VccQ
42 DQ8
41 Vss
40 RP#
39 DQMH
38 CLK
37 CKE
36 VccP
35 A11
34 A9
33 A8
32 A7
31 A6
30 A5
29 A4
28 Vss
150
152
154

Fig. 2

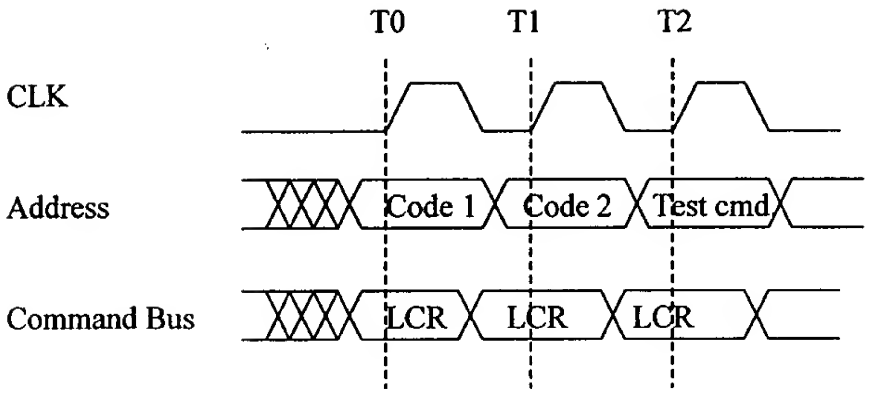
T0
T1
T2
CLK
Address
Code 1
Code 2
Test cmd
Command Bus
LCR
LCR
LCR

FIGURE 3